CLAIM AMENDMENTS

1. (Currently Amended) An interface for communicating between electronic components having multiple connection points, said interface comprising:

a circuit for a state machine to perform as a target and an initiator of a communication; and

a plurality of pins, connected to the circuit, ~~said~~ the plurality of pins corresponding to a set of target signals handling communication involving ~~the~~ an electronic component as a target and a set of initiator signals handling communication involving ~~the~~ an electronic component as an initiator,

wherein ~~said~~ the sets of target signals and initiator signals are ~~is~~ consistent with a virtual component interface protocol.

2. (Currently Amended) The interface of claim 1, wherein ~~each of~~ the ~~plurality of~~ pins are unidirectional and comprise at least one input pin and at least one output pin.

3. (Currently Amended) The interface of claim ~~2~~1, wherein the plurality of pins comprises equal numbers of input pins ~~is equal to the number of~~ and output pins.

4. (Currently Amended) The interface of claim ~~3~~1, wherein the set of target signals is symmetric with the set of initiator signals.

5. (Currently Amended) An electronic component comprising:

a circuit for a state machine to perform as a target and an initiator of a communication; and

a plurality of pins, connected to the circuit, ~~said~~ the plurality of pins corresponding to a set of target signals handling communication involving the an electronic component as a target and a set of initiator signals handling communication involving the an electronic component as an initiator,

wherein ~~said~~ the sets of target signals and initiator signals are ~~is~~ consistent with a virtual component interface protocol.

6. (Currently Amended) The electronic component of claim 5, wherein ~~each of~~ the ~~plurality of~~ pins are unidirectional and comprise at least one input pin and at least one output pin.

7. (Currently Amended) The electronic component of claim ~~6~~5, wherein the plurality of pins comprises equal numbers of input pins ~~is equal to the number of~~ and output pins.

8. (Currently Amended) The electronic component of claim ~~7~~5, wherein the set of target signals is symmetric with the set of initiator signals.

9-23. (Canceled).

24. (New) The interface of claim 1, wherein the set of target signals comprises receive and transmit signals, and wherein the set of initiator signals comprises receive and transmit signals.

25. (New) The interface of claim 1, wherein the circuit comprises a pin that can be tied to a logical 1 or 0 to select the state machine as a target or an initiator.

26. (New) The interface of claim 1, wherein the state machine can dynamically perform as the target and the initiator of the communication.

27. (New) The interface of claim 1, wherein the state machine can dynamically perform as the target and the initiator of the communication in response signals transmitted by one or both of the target and initiator.

28. (New) The interface of claim 1, wherein the set of target signals comprises a response, and the set of initiator signals comprises a request.

29. (New) The electronic component of claim 5, wherein the set of target signals comprises receive and transmit signals, and wherein the set of initiator signals comprises receive and transmit signals.

30. (New) The electronic component of claim 5, wherein the circuit comprises a pin that can be tied to a logical 1 or 0 to select the state machine as a target or an initiator.

31. (New) The electronic component of claim 5, wherein the state machine can dynamically perform as the target and the initiator of the communication.

32. (New) The electronic component of claim 5, wherein the state machine can dynamically perform as the target and the initiator of the communication in response signals transmitted by one or both of the target and initiator.

33. (New) The electronic component of claim 5, wherein the set of target signals comprises a response, and the set of initiator signals comprises a request.